IN THE CLAIMS

1. (Currently amended) A processor comprising:

scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements; and

traffic shaping circuitry coupled to the scheduling circuitry and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements;

wherein the scheduling circuitry is configured for utilization of at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to a transmission time slot and being configured to store at least one entry, the scheduling circuitry being operative in conjunction with the time slot table to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions between requests from the transmission elements for each of one or more of the time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

2. (Original) The processor of claim 1 wherein the time slot table is stored at least in part in an internal memory of the processor.

3. (Original) The processor of claim 1 wherein the time slot table is stored at least in part in an external memory coupled to the processor.

4. (Original) The processor of claim 1 wherein a given one of the locations in the time slot table stores an identifier of one of the transmission elements that has requested transmission of a block of data in the corresponding time slot.

5. (Original) The processor of claim 1 wherein one or more of the data blocks comprise data packets.

6. (Original) The processor of claim 1 wherein the established traffic shaping requirement is substantially maintained by linking together identifiers of transmission elements generating requests that collide for a given time slot, from a single entry in the corresponding table location, and then scheduling the requesting elements for transmission in the order in which they are linked.

7. (Original) The processor of claim 1 wherein the scheduling circuitry provides dynamic maintenance of the time slot table such that identifiers of requesting transmission elements are entered into the table locations on a demand basis.

8. (Original) The processor of claim 1 wherein identifiers of the transmission elements comprise a structure for allowing a given one of the transmission element identifiers to be linked to another of the transmission element identifiers.

9. (Original) The processor of claim 8 wherein in the event of a collision between multiple transmission elements requesting a given one of the time slots, an identifier of a first one of the requesting transmission elements is entered into the corresponding location in the time slot table, and that identifier is linked to an identifier of a second of the requesting transmission elements, with similar linking between the identifier of the second requesting transmission element and an identifier of any subsequent one of the requesting transmission elements, a linked list of the multiple requesting elements thereby being created for the corresponding location in the time slot table.

10. (Original) The processor of claim 9 wherein upon transmission of a data block from one of the requesting transmission elements in the linked list of elements, a determination is made as to whether there are any further elements linked to that element, and if there are any further elements, the identifier of the next such element is determined and that identifier is written into the corresponding location in the time slot table.

11. (Original) The processor of claim 1 wherein the scheduling circuitry maintains a set of pointers for the time slot table, the set of pointers comprising one or more of:

a current pointer pointing to the next location in the time slot table for which a data block will be transmitted;

an actual pointer pointing to the location in the time slot table corresponding to actual time; and

a free pointer pointing to the next location in the time slot table that is a free entry with no requesting transmission element assigned thereto.

12. (Original) The processor of claim 11 wherein in the event of a collision between multiple transmission elements requesting a given one of the time slots, a linked list of identifiers of the multiple requesting elements is created, and the current pointer continues to point to the corresponding location in the time slot table until each of the multiple requesting transmission elements has transmitted a data block.

13. (Original) The processor of claim 12 wherein the actual pointer advances by one table location for each of the data blocks transmitted.

14. (Original) The processor of claim 12 wherein the current pointer advances by one table location after each of the requesting transmission elements in the linked list associated with a given table location has transmitted a data block.

15. (Original) The processor of claim 12 wherein if the current pointer and the free pointer point to the same location in the time slot table and the actual pointer points to a different location in the time slot table, then the current pointer and the free pointer are both incremented to coincide with the actual pointer.

16. (Currently amended) ~~The processor of claim 12~~

A processor comprising:

scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements; and

traffic shaping circuitry coupled to the scheduling circuitry and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements;

wherein the scheduling circuitry is configured for utilization of at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to a transmission time slot, the scheduling circuitry being operative in conjunction with the time slot table to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions between requests from the transmission elements for each of one or more of the time slots, through the use of a linking of colliding transmission elements; and

wherein the scheduling circuitry maintains a set of pointers for the time slot table, the set of pointers comprising one or more of:

an actual pointer pointing to the location in the time slot table corresponding to actual time; and

a free pointer pointing to the next location in the time slot table that is a free entry with no requesting transmission element assigned thereto; and

wherein if the free pointer and the actual pointer point to different locations in the time slot table, and the actual pointer points to a location having a valid transmission element associated therewith, an identifier of that element is written to the location in the time slot table pointed to by the free pointer, and the identifier of that element is deleted from the location in the time slot table pointed to by the actual pointer, and both the free pointer and the actual pointer are incremented by one.

17. (Currently amended) ~~The processor of claim 12~~

A processor comprising:

scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements; and

traffic shaping circuitry coupled to the scheduling circuitry and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements;

wherein the scheduling circuitry is configured for utilization of at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to a transmission time slot, the scheduling circuitry being operative in conjunction with the time slot table to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions between requests from the transmission elements for each of one or more of the time slots, through the use of a linking of colliding transmission elements; and

wherein the scheduling circuitry maintains a set of pointers for the time slot table, the set of pointers comprising one or more of:

a current pointer pointing to the next location in the time slot table for which a data block will be transmitted;

an actual pointer pointing to the location in the time slot table corresponding to actual time; and

a free pointer pointing to the next location in the time slot table that is a free entry with no requesting transmission element assigned thereto; and

wherein a given requesting transmission element is assigned to a location in the time slot table in accordance with the following equation:

Assigned Time Slot = AP - (FP - CP) + Requested Time Slot Interval,

where AP denotes the actual pointer, FP denotes the free pointer, CP denotes the current pointer, and the requested time slot interval is the time slot interval requested by the requesting transmission element, such that when the actual pointer, free pointer and current pointer each point to the same location in the time slot table, the assigned time slot corresponds to the requested time slot interval.

18. (Original) The processor of claim 1 further comprising a transmit queue coupled to the scheduling circuitry and the traffic shaping circuitry, the transmit queue supplying time slot requests from transmission elements to the scheduling circuitry in accordance with the traffic shaping requirement established by the traffic shaping circuitry.

19. (Original) The processor of claim 1 wherein the processor comprises a network processor configured to provide an interface for data block transfer between a network and a switch fabric.

20. (Original) The processor of claim 1 wherein the processor is configured as an integrated circuit.

21. (Currently amended) A method for use in a processor for scheduling data blocks for transmission from a plurality of transmission elements, the method comprising:

establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements; and

scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more transmission time slots, utilizing at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to one of the transmission time slots and being configured to store at least one entry, and further utilizing a linking of colliding transmission elements and movement of at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

22. (Currently amended) An article of manufacture comprising a machine-readable storage medium for use in conjunction with a processor, the medium storing one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements, utilizing at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to a transmission time slot and being

configured to store at least one entry, wherein the one or more programs when executed implement the steps of:

establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements; and

scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more of the transmission time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.